

What is claimed is:

1. A semiconductor memory device, comprising:
a memory cell array having a plurality of memory cells, a plurality of word lines, and first and second bit lines;
5 an address decoder which decodes a received address signal, wherein the address decoder is coupled to the plurality of word lines;
a precharge control circuit that generates a precharge signal in response to a precharge enable signal and a precharge delay signal; and
a precharge unit that precharges the first and second bit lines in response to the
10 precharge signal.
2. The semiconductor memory device of Claim 1, further comprising a delay circuit which generates the precharge delay signal by delaying the precharge enable signal for a predetermined delay time.
3. The semiconductor memory device of Claim 2, wherein the precharge
15 control circuit comprises:
a NAND gate which receives the precharge enable signal and the precharge delay signal; and
an inverter which inverts the output of the NAND gate.
4. The semiconductor memory device of Claim 2, wherein the
20 predetermined delay time comprises the time that it takes the word lines to become enabled in response to a transition of the decoded address signal.
5. The semiconductor memory device of Claim 2, wherein the precharge unit comprises:
a first transistor which in response to the precharge signal precharges the first
25 bit line to a power supply voltage level;
a second transistor which in response to the precharge signal precharges the second bit line to a power supply voltage level; and
a third transistor which in response to the precharge signal equalizes the voltage of the first bit line and the second bit line.

6. The semiconductor memory device of Claim 5, wherein the first, second and third transistors are PMOS transistors.

7. The semiconductor memory device of Claim 2, wherein the delay circuit comprises a NOR gate which receives the precharge enable signal and an inverter which inverts the output of the NOR gate.

8. The semiconductor memory device of Claim 2, wherein the precharge control circuit generates the precharge signal by performing a logical AND operation on the precharge enable signal and the precharge delay signal.

9. The semiconductor memory device of Claim 1 wherein the address decoder is a row address decoder and wherein the decoded address signal comprises a row address.

10. The semiconductor device of Claim 9, wherein the precharge signal is disabled after one of the plurality of word lines is enabled in response to the decoded address signal.

11. The semiconductor device of Claim 1, wherein the precharge signal is disabled a predetermined time after the precharge enable signal is disabled.

12. The semiconductor device of Claim 11, wherein the precharge signal is enabled at substantially the same time that the precharge enable signal is enabled.

13. A semiconductor memory device, comprising:
a memory cell array having a plurality of memory cells, a plurality of word lines, and first and second bit lines;
an address decoder which decodes a received address signal, wherein the address decoder is coupled to the plurality of word lines;
a precharge control circuit which generates a precharge signal in response to the decoded address signal and a precharge enable signal; and
a precharge unit that precharges the first and second bit lines in response to the precharge signal, wherein the precharge signal is disabled in response to one of the plurality of word lines being enabled.

14. The semiconductor memory device of Claim 13, wherein the precharge control circuit comprises:

a NOR gate which receives the decoded address signals;

a first inverter which inverts the output of the NOR gate;

5 a NAND gate which receives the output of the first inverter and the precharge enable signal; and

a second inverter which inverts the output of the NAND gate to generate the precharge signal.

15. The semiconductor memory device of Claim 14, wherein the precharge unit comprises:

a first transistor which in response to the precharge signal precharges the first bit line to a power supply voltage level;

a second transistor which in response to the precharge signal precharges the second bit line to a power supply voltage level; and

15 a third transistor which in response to the precharge signal equalizes the voltage of the first bit line and the second bit line.

16. A semiconductor memory device, comprising:

a memory cell array having a plurality of memory cells, a plurality of word lines, and first and second bit lines; and

20 a circuit that is configured to disable the precharge signal that controls the precharging of the first and second bit lines in response to one of the word lines being enabled.

17. The semiconductor memory device of Claim 16, wherein the precharge signal is disabled after a predetermined delay time that is set as the time that it takes
25 the one of the word lines to become enabled in response to a transition of the decoded address signal.

18. A method of pre-charging a first bit line and a second bit line on a semiconductor memory device, the method comprising:

pre-charging the first and second bit lines in response to a precharge enable
30 signal transitioning to a first level until a predetermined time after the precharge enable signal transitions to a second level.

19. The method of Claim 18, wherein the predetermined time is comprises the time that it takes the word lines to become enabled in response to a transition of the decoded address signal.

20. The method of Claim 18, wherein the first level is a low logic level and
5 the second level is a high logic level.

21. The method of Claim 18, further comprising resuming the precharge of the first and second bit lines in response to the precharge enable signal transitioning back to the first level.

22. A method for pre-charging a first bit line and a second bit line of a
10 memory cell array, the method comprising:
decoding a received address signal;
generating a precharge signal in response to a precharge enable signal and a precharge delay signal;
pre-charging the first bit line and the second bit line in response to the
15 precharge signal; and
enabling a word line in response to the decoded address signal, wherein the precharge signal is disabled after the word line is enabled.

23. The method of Claim 22, wherein the precharge delay signal is generated by delaying the precharge enable signal for a predetermined time.

20 24. The method of Claim 23, wherein the predetermined delay time comprises the time that it takes the word lines to become enabled in response to a transition of the decoded address signal.

25. The method of Claim 22, wherein the precharge signal is disabled a predetermined time after the precharge enable signal is disabled.

25 26. A method for pre-charging a first bit line and a second bit line of a memory cell array, the method comprising:
decoding a received address signal;
generating a precharge signal in response to the decoded address signal and a precharge enable signal;

pre-charging the first bit line and the second bit line in response to the precharge signal; and

enabling a word line in response to the decoded address signal, wherein the precharge signal is disabled after the word line is enabled.

- 5 27. The method of Claim 26, wherein the precharge signal is disabled a predetermined time after the precharge enable signal is disabled.

28. The method of Claim 27, wherein the predetermined time is the time that it takes the word line to become enabled in response to a transition of the decoded address signal.

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